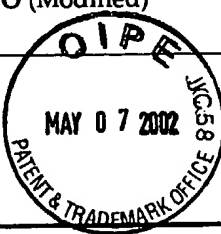


Substitute for Form 1449A/PTO (Modified)		Attorney Docket No.: 42390.P8533	Application Number: 09/608,856
Sheet 1 of 4		First Named Inventor: Jin Yang	Examiner: Unassigned
		Filing Date: June 30, 2000	Art Unit: 2123

## U.S. PATENT DOCUMENTS

Exam. Initial*	Cite No. <sup>1</sup>	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code <sup>2</sup> (If known)			
AB		5,469,367		Puri et al	11-21-1995	
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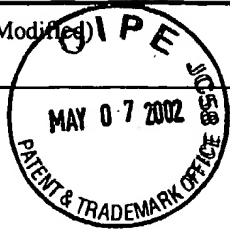
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Sheet 2 of 4	First Named Inventor: Jin Yang	Examiner: Unassigned
	Filing Date: June 30, 2000	Art Unit: 2123



**OTHER ART - NO PATENT LITERATURE DOCUMENTS**

Examiner Initials*	Cite No <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	Translation <sup>2</sup>
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Sheet 3 of 4		First Named Inventor: Jin Yang	Examiner: Unassigned
		Filing Date: June 30, 2000	Art Unit: 2123

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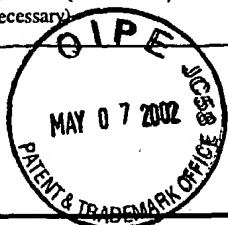
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Sheet 4 of 4	First Named Inventor: Jin Yang	Examiner: Unassigned
	Filing Date: June 30, 2000	Art Unit: 2123



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AS		JAIN, A., "Formal Hardware Verification by Symbolic Trajectory Evaluation," <i>Carnegie Mellon University Ph.D. Dissertation</i> , July 1997	
		JAIN, S. et al, "Automatic Clock Abstraction from Sequential Circuits," <i>Proceedings of the 32<sup>nd</sup> ACM/IEEE Conference on Design Automation</i> , January 1995	
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Substitute for Form 1449/PTO (Modified) (use as many sheets as necessary)		Attorney Docket No.: 42390.P8533	Application Number: 09/608,856
Sheet 1 of 1		First Named Inventor: Jin Yang	Examiner: Unassigned
		Filing Date: June 30, 2000	Art Unit: 2123
<b>OTHER ART - NO PATENT LITERATURE DOCUMENTS</b>			
Examiner Initials*	Cite No <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	Translation <sup>2</sup>
AB		BRADLEY, J., et al., "Compositional BDD Construction: A Lazy Algorithm," Department of Computer Science, University of Bristol, UK, April 6, 1998	
↓		BURCH, E. M., et al., "Symbolic Model Checking for Sequential Circuit Verification," <u>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</u> , Volume 13, Issue 4, April 1994, pp. 401-424	
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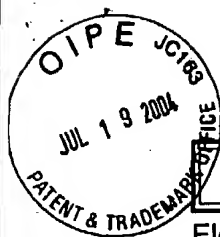
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## ELECTRONIC INFORMATION DISCLOSURE STATEMENT

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Title of Invention	Methods for performing generalized trajectory evaluation																																		
<p>Application Number: 09/608856 </p> <p>Confirmation Number: 2493</p> <p>First Named Applicant: Jin Yang</p> <p>Attorney Docket Number: 42P8533</p> <p>Art Unit: 2123</p> <p>Examiner: Samuel Broda</p> <p>Search string: ( 5870590 or 6484134 ).pn.</p> <p><b>US Patent Documents</b></p> <p>Note: Applicant is not required to submit a paper copy of cited US Patent Documents</p> <table border="1"><thead><tr><th>init</th><th>Cite.No.</th><th>Patent No.</th><th>Date</th><th>Patentee</th><th>Kind</th><th>Class</th><th>Subclass</th></tr></thead><tbody><tr><td></td><td>1</td><td>5870590</td><td>1999-02-09</td><td>Kita et al.</td><td></td><td></td><td></td></tr><tr><td></td><td>2</td><td>6484134</td><td>2002-11-19</td><td>Hoskote</td><td></td><td></td><td></td></tr></tbody></table> <p><b>Signature</b></p> <table border="1"><thead><tr><th>Examiner Name</th><th>Date</th></tr></thead><tbody><tr><td></td><td>9/18/04</td></tr></tbody></table>								init	Cite.No.	Patent No.	Date	Patentee	Kind	Class	Subclass		1	5870590	1999-02-09	Kita et al.					2	6484134	2002-11-19	Hoskote				Examiner Name	Date		9/18/04
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